Analysis of Solutions Concerning Various Power Optimization Techniques for Low Power Embedded Systems

A. Nazarudeen, P. Jayaprakash

Abstract - The proliferation of Anywhere-Anytime intelligent portable computing devices and the Internet of Things (IoT) has created an increasing demand for low power embedded systems, which has resulted in the fabrication of tiny high-speed processors with higher packaging density and powerful computing capabilities. These portable devices are expected not only to be small, lightweight and cool but also to provide incredibly long battery life. This requirement has presented significant challenges for managing the power in low power embedded systems, and it has shifted the designers' focus from traditional constraints to power consumption. Based on the various power profiling studies conducted, the embedded researchers have proposed many solutions and methodologies in terms of new power saving architectures as well as power optimization techniques. This paper analyzes in detail the various studies conducted and solutions suggested by the researchers for optimizing the power consumption in embedded systems.

Keywords -Embedded systems, power optimization techniques, Dynamic power, leakage power, Voltage and frequency scaling.

1 INTRODUCTION

Power consumption has become one of the main design metrics among other metrics used to characterize the quality of the embedded system design. Nowadays, mobile computing devices are packed with thousands of processors and millions of transistors in a single chip to reduce the size and increase the system performance. The frequency of the system clock has also been increasing consistently to enhance the speed of operation. This increase in frequency indirectly aids the power consumption and thereby decreases the battery life. Also, it affects the cooling and the packing cost of the system. Since high-performance computing leads to increased power dissipation in the system, designing high-performance portable computing devices with extended battery life has always been a major challenge for the designers. A lot of research has been done and novel solutions have been proposed by the academic and industrial research community to address the critical issue of power consumption at different levels of the embedded system architecture such as design, gate, register and instruction, memory, operating system,software, application, peripherals, and power supply.As more and more portable computing devices are becoming part of everyday life, the research for optimizing the power has also been dominating, and it will continue to be the main focus in the embedded system design. Since there are thousands of publications in literature related to this topic, it is not possible to do justice to all these research works. So to limit the scope of this analysis, we review only the research concerning some of the most commonly used optimization techniques. Although several techniques can be applied at more than one architectural level, it is not possible to apply all techniques simultaneously. However, possible scenarios are outlined in this paper. First we outline the mainfactors that affect the power consumption, followed by importance of power management, synopsis of most commonly used optimization techniques, and finally wereview the research papers published recently in the world conference proceedings and journals concerning various power optimization techniques.

- A. Nazarudeen, Research Scholar,
  Department of Electronics,Banasthali University, Rajasthan, India
  email: nazraziz@gmail.com.
- P. Jayaprakash, Professor & Head,
  Mohandas College of Engineering & Technology, Trivandrum (affiliated to APJ Abdul Kalam Technological University, Kerala,) India, e-mail: jpavithran2011@gmail.com

2 FACTORS AFFECTING POWER CONSUMPTION

In an embedded system, a base hardware platform (SoC) executes the system and application software, and interacts with the peripherals through communication channels or buses. Therefore, the total power consumption in an embedded system is the sum of power consumed by all parts of the system. It is well known that the SoC is implemented using CMOS technology, and the dynamic power (P_{DY}) and the static or leakage power (P_{ST}) are the two primary components of the total power (P_T) in a CMOS circuit. P_{DY} refers to the power dissipated when the circuit is normally operating and produces a meaningful output. P_{ST} is the power dissipated whenever the processing elements are switched on, but no active computations are carried out. P_{DY} can further be sub-divided in two components: switching power (P_{SW}) and short circuit power (P_{SC}). In a well-designed circuit, the

short circuit power is typically negligible compared to the total power. The leakage current is not a severe problem in conventional digital logic designs as it is of the order pico-ampere. However, with the current deep-micron technology it can be as large as switching current and hence becomes one of the main concerns. Thus, the total power consists of mainly two components $P_{SW}$and $P_{ST,}$ which can be modeled by the following equations;

$$P_{SW} = 0.5\ \alpha\ f\ C\ V^2 \qquad 2.1$$

$$P_{ST} = I_L\ V \qquad 2.2$$

Where α is the activity factor, **f** is the frequency of the system, **V** is the supply voltage, **C** is the load capacitance, and $\mathbf{I}_L$ is the leakage current which originates from various phenomena [2],[3]. Thus, a designer tries to scale these parameters at the technological, architectural and system level to minimize the power consumption. However, there are limitations for scaling these parameters as the performance of a CMOS circuit also largely depends on these parameters [4].

Sometimes, designers concentrate too much on processing and memory units, ignoring the power consumption in peripheral devices. However, peripheral devices such as displays, audio/video devices, keyboards, sensors, network devices, and other I/O devices and their interconnections consume a significant fraction of the total power. Hence, the designers must consider the power consumption in peripherals also into account while addressing the power issues [6].

The methods of software implementation also affect the power dissipation of base hardware and peripheral devices. For example, the choice of operating system calls, memory access patterns, the number of instructions in the program, and the power efficiency of compiled codes play significant roles in the overall power dissipation of the systems because all these factors affect the switching activity of the various units in the system. Hence, the designers must use optimized software for minimizing the power in hardware, which necessitates a tradeoff between the hardware and software [5],[60]

3 IMPORTANCE OF POWER MANAGEMENTS

The power consumption of low power portable devices has to be limited because of many constraints such as; the world's ICT ecosystem is nowadays consuming significant share of the world electricity generation [57], the workload of cell phones increases while keeping a fixed battery capacity, and to achieve the goal of green computing the C_{O2} emissions generated by electronics and ICT systems should be minimized. The following section briefly explains the importance of minimizing power consumption in low power portable devices [1].

3.1 Limited Size and Battery

Power consumption is a crucial issue in battery-operated low power lightweight embedded systems because power consumption causes heating which is not acceptable in several applications such as cell phones and other wearable embedded systems. The size of the system also limits the amount of heat dissipation. So low power consumption reduces heat dissipation and enables to use small sized batteries which further helps to reduce the weight, size, and cost of the whole system. Also, an increase in power consumption decreases the life of the battery and the duration of operation of the system. There is a remarkable growth in the CMOS technology regarding device density and computing power. However, the battery technology has not undergone a similar growth. It created a gap called *battery gap* which also forces the need for power minimization in low power devices [7].

3.2 Ensuring Reliability and Long Life Cycle

Power dissipation has a harmful effect on the reliability and the life cycle of embedded systems. It may be crucial for medical devices and mission-critical systems because failure or malfunction of life critical systems based on embedded processors may result in serious injury or death to humans or severe damage to equipment. Studies show that a fifteen degree Celsius rise in temperature increases the device failure rates by up to a factor of two [58]. So, the failure rate of the embedded systems can be decreased by reducing the temperature which can be achieved by reducing the power consumption.

3.3 Meeting Performance Requirements

Managing power consumption in an embedded system is increasingly important as more and more devices are becoming Internet-connected smart devices (IoT applications) to execute resource-intensive applications such as multimedia processing, net browsing, and wireless data streaming [8]. So the modern embedded processors use many complex features such as multi-cores, and multi-level caches to meet the performance requirements [9]. Hence, the design of embedded systems must be optimized for low power consumption and high-performance to meet the demands of these modern trends.

3.4 Power Challenges Posed by CMOS Scaling

The technological advancements have resulted in ever smaller dimensions of transistors, fabrication of CMOS/VLSI circuits with higher packaging density, and high-speed tiny processors with powerful computing capabilities. This reduction in device dimensions increases the computing density and increases the leakage current and the power consumption [59]. Since the power consumption primarily constrains the processor performance, this challenge has to be

addressed seriously to avoid further scaling of system performance [60].

3.5 Trends in Usage Pattern of Portable Systems

In recent years, low power embedded systems have become the key platform for the mobile computing applications such as net browsing, imaging, video streaming, and wireless data streaming, and due to these trends, embedded systems have become ubiquitous. It has been reported that the number of mobile computing devices has become nearly equal to the population of the earth and the world's ICT ecosystem is nowadays consuming 10% of the world's electricity generation [1][57]. Thus the large user-base of mobile computing devices makes the share of the total power consumption very high. So, power management has become critical for mobile computing devices.

3.6 Achieving the Goals of Green Computing

Green computing refers to the environment-friendly use of computer systems, which means that the implementation of the best practices and technologies aim to reduce the resource consumption and overall carbon footprint. It has been estimated that the ICT contributes nearly 3% of the overall carbon footprint [10]. Thus, power minimization is highly important in achieving the goals of green computing.

4 SYNOPSIS OF COMMONLY USED POWER OPTIMIZATION TECHNIQUES

TABLE 1
Synopsis of power optimization techniques

Technique	Brief Description
Gate sizing (GS)	Changing the size of the gate changes the load capacitance and hence changes the switching current. Upsizing reduces the dynamic power, improves the slew time and downsizing reduces the leakage power [11],[12],[13],[17],[19].
Logic re-structuring	Optimizes the dynamic power at gate level by moving high activity logic to the front and low activity logic to the back [14],[15],[16]
Operand Isolation	Isolates redundant operations and prevents switching activity of inactive data path elements [17],[18],[19]
Substrate Biasing	Substrate or appropriate well is dynamically biased to raise the transistor threshold voltage in active mode to reduce the leakage power [20],[21],[22]
Multiple threshold voltages (MTV)	Utilizes gates using transistors with different switching threshold voltage to reduce the leakage power while maintaining the timing constraints – lower leakage power at higher threshold but slower and higher leakage power at lower threshold but faster [23],[24],[25],[38],[47]
Clock Gating (CG)	Disconnects or disables the clocks to the unused circuit blocks in the system to save dynamic power [26],[27],[28],[29].
Memory partitioning	Partitions the memory into several blocks and shut off the unused blocks to save the leakage power during the idle period [30],[31],[32].
Bus Segmenting	The bus is split into several segments, and only the buses essential for access are activated to avoid the powering of the entire bus system [33],[34]
Bus encoding	minimizes the dynamic power consumption by reducing the switching activities in the bus using bus inversion technique [35],[36],[37]
Multiple supply voltages (MSV)	Uses different fixed supply voltages for different blocks (called voltage island) in the chip based on their performance requirements – high voltage for high-performance block and low voltage for low-performance blocks [23],[38][39],[40],[47]
Dynamic Voltage Scaling/ Dynamic Voltage and Frequency Scaling (DVS/ DVFS)	Different blocks in a chip operates at variable voltages/different blocks in a chip operates at variable voltages and frequencies based on the performance requirements of the target application to reduce the dynamic power [13],[21],[41], [42],[43],[53]
Power gating (PG) or Power Shut-Off(PSO)	Temporarily shuts off the power to part of the circuit blocks that are not in use (or in sleep, deep-sleep, standby mode) and turned on when the blocks are required for operation – reduces a significant amount of leakage power [18],[44],[45], [46],[47]
Hardware Acceleration	Uses additional hardware elements to speed-up or to enhance the performance of the system. This additional hardware can be shut off when not needed [48] – [50]
Selective Peripheral Clocking	switches the peripheral devices that are not in use to reduce the static power consumed by the peripheral devices [51],[52]
Configuring Power Delivery Network (PDN)	Employs adjustable DC-DC converter to improve the power conversion efficiency of the power delivery network (PDN) [53],[54],[55].

5 RELATED WORK

Wang et al. 2011 [11] propose a heuristic gate sizing algorithm for glitch power reduction for a semi-custom

design which minimizes the total power metric of a circuit. The experimental results on eight ISCAS85 benchmark circuits and five real industrial circuits show that this algorithm can save more than 34% of average glitch power and 15.5% of average total power. Besides theses power savings, it reduces the area by 3.5%. These achievements are more than those using conventional gate sizing algorithms

How-Rern et al. 1995 [12] introduce a gate sizing approach to reduce the power in circuits that have already satisfied the timing constraints. In this method, the gates on non-critical paths are replaced with smaller templates for reducing power dissipation. A path-oriented time slack calculation algorithm with sensibility taken into account is proposed for power reduction using single and multiple gate sizing. Results on a set of circuits from MCNC (Microelectronics Center of North Carolina) benchmark set demonstrate that this power reduction algorithm can reduce about 10% more power, on the average, than a previously proposed gate sizing algorithm.

Chunhong et al. 2000 [13] present an algorithmic approach to using the voltage-scaling (VS) and gate-sizing (GS) simultaneously for power minimization without violating the timing constraints. The algorithms manage the power under the given time constraints by dealing with the Maximum-Weighted-Independent-Set (MWIS) problem on transitive graphs, and it is demonstrated that the VS approach is related to the power supply voltage, while GS technique depends on the underlying gate library. It has been shown that the proposed simultaneous voltage-scaling and gate sizing provides globally useful solutions with inexpensive computation cost. The implementation results show that the average power reduction ranges from 23.3% to 56.9%.

Senthilkumar et al. 2016 [14] analyze the stack effect and propose a combined device sizing and logic restructuring approach and verify that there is no stack effect among FinFETs. The experimental setup using industrial standard 7nm FinFET shows that the proposed approach can reduce power by 57% and area by 37.5% with delay penalty of 42.2% compared to the conventional logic method. Since this approach is free from stack effect, they propose a high Fan-in gates structure and achieve a reduction in input capacitance

Quang et al. 2010 [15] present a binary decision diagram (BDD) - based decomposition algorithm to restructure the circuit and expose possible control signals that would maximize power saving and use the integer linear programming (ILP) to select the optimal set of logic signals for the circuit. They show that the constraint matrix is totallyuni-modular, and solve this selection problem optimally using linear programming. Compared to the original and non-structured circuits, this approach gives 9% more saving of dynamic power for small/medium circuits and an average of 19% dynamic power saving with 9.3% area overhead larger circuits.

Hosung et al. 2008 [16] implement a timing-driven logic restructuring at the physical level. They propose a choice tree construction and a new dynamic programming algorithm for optimizing the performance. The implementation in FPGA domain shows promising results – average 14.8% reduction in clock period compared to timing driven VPR (Versatile Place and Route) and 6.6% compared to basic embedder.

Jun et al. 2007 [17] utilize clock gating technique to minimize the unnecessary power consumption in logic blocks and operand isolation to minimize the power in data-path by reducing the unnecessary switching. Implementation with DSP as the target platform has shown a switching power saving of 27.64% without any critical path delay and with a little increase (2.1%) of area overhead.

Banerjee et al. 2006 [18] introduce an operand isolation techniques (at the block and bit level) based on power gating that minimizes leakage power and significantly lowers the overhead associated with the existing isolation circuits. The proposed integrated synthesis methodology automates the application of the operand isolation techniques at RT level to reduce the power consumption and delay. Simulation results show that the proposed techniques based on power gating can achieve minimum 40% reduction in power consumption compared to an original circuit with minimal area overhead of 5% and a delayed penalty of 0.15%.

Fábio et al. 2016 [19] present a hardware architecture for the binary arithmetic encoder (BAE) of the Context-adaptive binary arithmetic coding (CABAC) for low power design techniques such as clock gating and operand isolation. The techniques were incorporated after careful analysis based on the behavior of CABAC inputs for real video sequences. Implementation is done on a four-cores BAE structure by applying the techniques mentioned above in a specific part of the hardware to provide high performance. The results have shown that power reduction in the range of 25 to 40% can be achieved with this technique.

Youssef et al. 2003 [20] explore the usage of reverse bulk node voltage to resolve the tradeoff between speed and noise immunity which is greatly affecting the leakage power. The effect of the bulk node voltage is studied and compared to the effect of increasing the keeper size and found that reduction in bulk node voltage causes a significant saving in the leakage power while maintaining the gate delays. Managing both the keeper and reverse bulk voltage simultaneously will lead to further savings in the leakage power with reasonably good noise margins. Experimental results have shown that a 50%

reduction in active leakage power and 40% saving in gate delay is achieved with this approach.

Po-Kuan et al. 2006 [21] use a power-aware compilation methodology that targets both dynamic voltage scaling (DVS) and adaptive body biasing (ABB) capabilities. This approach has the unique advantage of jointly optimizing the dynamic and leakage power dissipation. Also, considering the penalty of delay and energy in switching between processor modes, this approach generates code with minimum power dissipation under deadline constraints. The optimization results show that an average of 13.69% and 25.81% power improvement compared with DVS optimized and original code, while the maximum improvement was respectively 18.26% and 27.73%.

Seidai et al. 2012 [22] implement a simpletechnique, called step-wise sleep depth control that selects the best depth among the multiple sleep depths provided. This scheme automatically applies deeper depth in a step-by-step manner after an idle state starts and it significantly minimizes the leakage power. Also, propose an approach for optimizing the control parameters of the sleep control scheme based on the program behavior and temperature. The experimental outputs that this technique applied to body biasing circuit saves the net leakage power up to 43.00% for FPAlu (benchmark) at 1.0GHz compared to conventional RBB.

Gurfran et al. 2013 [23] propose a new high-performance multi-threshold voltage (MTV) level converter for a MSV system which provides the level up conversions for the various input voltage levels and compared with previous level converters. The proposed level converter is implemented with Cadence Virtuoso tool in UMC 180nm standard CMOS technology. The simulation results show that this level converter offers power reduction up to 38.1% and is up to 21.99% faster than the current voltage level converters. Also, the proposed converter shows an overall improved performance by exhibiting up to 14.31 to 50.88% less power delay product (PDP) than the existing level converters.

Frank et al. 2004 [24] present a new mixed voltage technique for CMOS, which uses multi-threshold voltages within a logic gate. Initially, a circuit is designed which consists of only one type of gate and later developed a 4-bit adder design with a supporting algorithm for the optimal distribution of the gates. This new MTV technique allows saving of leakage power up to 40% while maintaining the performance.

Feng et al. 2005 [25] propose an automatic implementation of both gate sizing and MTV techniques using a mixed linear programming model (called *MLP-exact) to* minimize the total active power consumption of a circuit. This technique considers both local as well as global optimality. Also, they describe an efficient way to solve the MLP model, called *MLP-fast*, which exhibits 1 or 2 folds of magnitude speedup for most benchmark circuits, with 3% power overhead. The experimental results show that the designs generated by *MLP-fast* consume 30% less power than conventional methods.

Maria et al. 2016 [26] present a ring counter with clock gated by the C-elements which eliminates the excessive data transition without increasing loading on the global clock signal during the write operation in CMOS SRAM cell. The gated-driver tree technique used for the clock distribution networks can eliminate the power wasted on drivers that need not be activated. Experimental results indicate that the proposed architecture consumes only about 13% to 17% of the conventional SRAM-based delay buffers in 0.18- μm CMOS technology.

Pritam et al. 2016 [27] employ the clock gating technique, incorporating Leakage Control TransistOR (LECTOR) mainly in the sequential logics of an IC. The proposed logic implemented on a D flip-flop using the PTM technology (predictive technology model) at 1.1.V and is simulated with an operating clock frequency of 1.25GHz. The simulation results show 10.43% saving in dynamic power with a loss of 24.76% and 4.93% on static and average power respectively with the 65nm approach of proposed logic. Also, there is a gain of 1.01% in delay and a latency gain of 8.34%

Doron et al. 2017 [28] combine the data-driven clock gated (DDCG) and multibit flip-flops (MBFFs) techniques into a single grouping algorithm for the power reduction in the low-power system (usually these low-power design techniques are treated separately). The results of implementation show that compared with conventionalFFs designs, a practical design utilizing the relationship between the MBFF multiplicities to FF data-to-clock toggling probabilities achieves power savings between 17% and 23%.

Jie et al. 2017 [29] propose a cache power optimization technique based on compare-based self-adaptive clock gating (CACG). This method saves cache power efficiently by gating the clock. The actual experimental measurements of a SoC chip using CACG show that this approach can save about 30.3% of total power reduction without affecting the performance and with negligible implementation cost.

Mathew et al. 2011 [30] propose a run-time and adaptive instruction cache partitioning approach which leverages user-configurable cache architectures. This method enables to achieve power and performance through conscious adaptive mapping of instruction caches to tasks in dynamic workloads sharing trough preemptive multitasking of a processor core. A significant amount of leakage and dynamic power reductions can beachieved with only a negligible and system-controlled impact on performance. The experimental results show that the

proposed dynamic cache partitioning approach can save 50% to 80% dynamic and leakage power for the on-chip instruction cache memory.

Alice et al. 2010 [31] propose a trace-based method to design two partition array caches with a size constraint that introduces a metric that quantifies access concentration so as to minimize the average memory access energy-delay product. The test results show that for some applications the splitting of cache improves average memory access energy-delay product, energy, and time. Also, if necessary, parallel accesses to cache partitions is possible, and it can improve these metrics further for some applications. For an 8K-byte cache, the trace-based split cache designed for an MPEG decoder exhibits an average access energy-delay product improvement of 50%, even assuming no parallel accesses.

Jason Cong et al. 2009 [32] present an automatic memory partitioning technique which can efficiently improve the performance and reduce power consumption of pipelined loop kernels for a given performance constraints. This scheme has two steps; in the first step, a cycle accurate scheduling information is considered to meet the hard constraints requirements of memory bandwidth, specifically for hardware designs of synchronized nature. The experimental results show that on a set of real-world designs, an average six-fold performance improvement with a moderate increase in the area about 45% on average. In the second step, the memory bank is further partitioned to reduce the dynamic power of the final design. This approach can statically compute the frequency of the memory access in polynomial time, and the experimental results show that power reduction of about 30% is achievable with the same set of benchmarks.

Hua et al. 2004 [33] present a methodology for reducing power in the bus of a memory dominated system. This method combines a bus segmentation approach and activitydriven placement of the memories for the interconnect to localize the switching activity of the wires to minimize the associated wire capacitance of the memory bus. Experimental results show this approach can reduce the bus power consumption by a factor of 2.8 for a real life design while maintaining the normal performance.

Suresh et al. 2005 [34] introduce a method to perform both bus segmentation and bus frequency assignment to each bus segment simultaneously while optimizing the performance and power consumption of the embedded system. This method uses a genetic algorithm and develops an appropriate cost function which optimizes the power consumption and performance. The experimental results show that an average of 60% power reduction can be achieved using this method compared to a single shared bus architecture.

Dinesh et al. 2003 [35] propose a frequent value encoding (FVE) techniques forreducing the data bus switching activity leading to more reduction in the dynamic powerconsumption. This technique exploits bit-wise temporal and spatial locality in the databus values by proposing three new schemes and five new variations without using theadditional external control signal to captures bit-wise locality to efficiently encode data values. Implementation of embedded and SPEC applications shows that the overall average switching is reduced by 53% compared to an un-encoded data, which is 11% higher than the conventional FVE scheme.

Shidi et al. 2011 [36] present a new bus encoding technique which can reduce the dynamic power consumption on the bus. This approach can also eliminate effectively the crosstalk problems in the bus partitions as well as inter-partitions by analyzing, formulating, and solving the problem of minimizing the self and coupled transition activities in the context of self-shield encoding. The experimental results show that this coding technique can totally avoid the crosstalk problems and reduce the dynamic power up to 63% for 24-bit buses.

Mohammad et al. 2011 [37] introduce a power-aware adaptive bus encoding method (simply PABEM) based on Huffman algorithm which relies on a change in adaptive Huffman coding algorithm. This approach results in reduced bit transitions of the output code, words reduced the numbers of switching activities and thereby reduce the power consumption. Evaluations using 30 text files of different sizes show that it can reduce the numbers of bit transitions and bus power consumption up to 49% and 46% compared to adaptive Huffman coding respectively.

Anish et al. 2008 [38] propose a method called threshold voltage control through multiple supply voltages (TCMS). This approach is significantly different from the conventional MSV approach. The variation of the van Ginneken's classic dynamic programming for solving the problem of power-optimal TCMS buffer insertion on a given routing tree is described in this approach. Also, a circuit design for a FinFET buffer using TCMS is developed. Experimental results show that TCMS can provide power savings of 50.41% with a device area savings of 9.17% compared to the dual supply interconnect synthesis scheme.

Marco et al. 2013 [39] introduce a Level Shifter (LS) to commute from one voltage domain to another for a Multiple Dynamic Supply Voltage (MDSV) approach to reduce the dynamic power. Normally LS inserted during the synthesis will degrade the performance and power, particularly in low power modes. However, the proposed approach dynamically turns off the idle LS and use alternate path for the current according to the power modes of the regions where net are connected. This

approach allows to save more than 35% power consumption and reduce the delay by 30%.

Harry et al. 2016 [40] present a by-pass circuit for multi-voltage scaling systems at different critical paths with blocks having the same voltage in specific operating conditions are grouped together. The key idea was to avoid performance and power losses where high-speed operation is required, by-passing the interface circuits to alleviate the timing issues and at the same time supporting multi-voltage scaling. The proposed circuit is simulated under different operating scenarios at a 32 nm technology node can save the power consumption up to 52% compared with conventional level-up/level-down shifters with an enhance speed of 89% while the interfaced block operates at the same frequency.

Ying-Xun et al. 2011 [41] introduce a parallel decoding process with DSP for power saving in a low power heterogeneous multicore SoC at the system level by combining multi-core scheduling and a DVFS mechanism. It provides a highly efficient multimedia decoding mechanism which decreases the system power usage through scheduling, correcting calculations, and resolving the multimedia data dependency issues. This mechanism, implemented on the Android system shows that there is a decrease of 36.2% to 41.9% power consumption.

Changyi et al. 2016 [42] propose a novel dynamic energy saving scheduling algorithm for sporadic tasks in real-time embedded systems (DESSAST-RTES) based on early deadline first (EDF) approach. Considering the difference between the real execution time (RET) and the worst-case execution time (WCET), this technique can dynamically scale processor frequencies with the RET, while guaranteeing that all tasks would not miss their deadlines. The experimental results show that the DESSAST-RTES consume 11.39%-52.23% less energy than existing DVS algorithms for sporadic tasks (DVSST, CC-DVSST, and DSTLPSA).

Anas et al. 2016 [43] propose some algorithms for the middleware which perform computation offloading for the sporadic and frame-based RT tasks to reduce the workload of the embedded systems and save power by offloading the tasks to a powerful server. This methodology was evaluated using a surveillance system and synthesized benchmarks, and the simulation results show that this scheme can save nearly 40% of the total power consumption compared to the case that of all tasks are executed locally with maximum processor speed.

Ricardo et al. 2016 [44] present an efficient hardware-software solution for reducing the leakage power consumption in a Java Optimized Processor (JOP) using a memory power management strategy. This method combines a power gating scheme and a multi-bank memory architecture for effective run-time power management to reduce the leakage power consumption of the heap memory characteristic of Java processors. The test results of this method on JOP using both Xilinx FPGA and ST Microelectronics 65nm CMOS standard cell library show that this method can save at least 50% leakage power with less than 0.1% of the hardware overhead with negligible performance overhead.

Ye-Jyun et al. 2015 [45] propose two memory access-aware approaches at system-level for the optimization of performance and leakage optimization. First, a Hierarchical Memory Scheduling (HMS) approach which improves the system performance by minimizing the interference among the memory requests within the inter-IP and application. Second, a memory based mechanism for MPSoCs to maximize the power-gating opportunity at a finer granularity, mainly focusing on the memory idleness due to access delay. The test results show that the proposed approaches improve power savings by 70% compared to conventional power gating based on time-out approach and with HMS, the power-gating efficiency is high as high as 76%, compared to conventional power gating with First-Come-First-Serve (FCFS) memory schedule. Also, the proposed HMS memory scheduling policy improves system throughput by 42% compared to FCFS and by 21% compared to First-Ready First-Come-First-Serve (FR-FCFS) on an MPSoC for mobile phones.

Michael et al. 2011 [46] present a method of using Nano-Electro-Mechanical-System switches (NEMS) for power gating the idle functional unit of an embedded processor. This approach identifies and quantifies the sources of power overhead such as charge pump, switch capacitance, and functional units. The accurate cycle simulation was carried out to find the cycle count overhead of the delay of a mechanical switch and the results show a saving of 26.1% of the total energy using a simple hardware scheduler and 29.4% using a conventional idlescheduler with an idle mechanical delay of 5% increase in cycle count.

Rahul et al. 2016 [47] propose a low power light-weight distributed power-gating router for the network on chip (NoCs) called, Fly-Over (FLOV). This FLOV power gating routers can be attached to the cores that are powered-down without global network information, but still, can ensure network connectivity. A handshake protocol is used for seamless router power gating in conjunction with a dynamic routing algorithm which provides thebest effort minimal path without any need for global network information. Performance evaluations using synthetic and real workloads show that FLOV achieves better NoC with average power saving of 15.9% with an average 19.2% latency reduction.

Vazgen et al. 2016 [48] present a combination of three optimization techniques such as multi-voltage, multi-threshold and power gating to reducing the dynamic and static power consumption of an Open RISC processor.

The experimental results showthat the combination of power gating, multi-threshold, and multi-voltage design approach is efficient by more than17% of saving power of an Open RISC 1200 processor with acceptable area penalty of 15%.

Giuseppe et al. 2016 [49] propose an alternative and novel approach to provide OpenVX support in heterogeneous systems including an MCU and a parallel accelerator. This method is an extension to the original OpenVX model to support static management of application graphs, which provides a lightweight support to execute static graphs in a resource-constrained environment. The experimental results show that this approach drastically reduces the memory footprint by 68% and the required bandwidth by 10%. Moreover, there is an average three-fold execution speed-up and a two-fold energy efficiency compared to the baseline implementation.

Renzo et al. 2016 [50] present a flexible, energy efficient and performance scalable convolutional neural networks (CNN) engine, the first ASIC design exploiting recent results on binary connect CNNs, which simplifies the complexity of the design. This approach uses simple complement operations and multiplexers as accelerators in place of the fixed-point MAC units with no hurt in accuracy.To improve the energy efficiency and extend the performance scalability of the accelerator, latch-based SCMs for on-chip data storage is designed supported with three different kernel sizes (3x3, 5x5, 7x7), to increase the flexibility - making it suitable for implementing a wide variety of CNNs. This method leads to a reduction of 29% in energy efficiency without significant reduction in performance.

Altera Corporation, 2009 [51] demonstrate the power savings techniques that the designers can achieve by using HW accelerators. A low-cost design example has been developed using an FPGA platform – an Altera EP3C25F324 with 25K LEs, 50-MHz, 66 M9K memory blocks, 16 multiplier blocks 18x18), and four PLLs. The Mandelbrot algorithm is used for calculating fractals and execution, using the Altera® Nios® II embedded processor. Although the size of the FPGA is small, the processor takes only a portion of its space, and this makes room for implementing additional hardware to accelerate the execution of the algorithm. The experimental results with processor alone and the processor with as many as five hardware accelerators have shown significant improvements in performance and savings of power; Baseline tests show that using processor alone (Nios II processor) require 435 million clock cycles to complete the processing of one Mandelbrot frame and with addition of a single hardware accelerator brought the requirement down to 4.9 million clock cycles (nearly 90-fold improvement in performance) without a significant increase in power demand. Adding four more accelerators shows an incremental improvement in performance as much as 435 fold of the processor alone and the power consumed by the additional accelerators was only 90% greater than the CPU alone. However, with reduced system clock frequency (80 MHz) and accelerator clock frequency (5 accelerators running at 1 MHz) increases the system performance by six fold with a saving of 55 % of the total power compared to executing the process with processor alone.

Ozgur et al. 2004 [52] introduce a methodology for estimation of power dissipation in peripherals such as video and audio devices. A cycle-accurate simulator and profiler capable of simulating peripheral devices are introduced along with I/O communication protocols such as DMA access, polling, and I/O interrupts. Also, optimize an audio driver for an MP3 audio decoder application using the power simulator and estimator. The optimization results show that a power reduction of 44% of the total power consumption can be achieved with the audio optimizer.

Andrea et al. 2003 [53] implement a new methodology for minimizing the power consumption of wireless portable devices - a new power management infrastructure for the Linux operating system based HP's SmartBadge4 wearable computer. The experimental results show that energy savings of up to 50% can be achieved with the power management implemented as a part of the 802.11b standard.

Behnam et al. 2007 [54] design an efficient low voltage power delivery network (PDN) for SoC with DVS capability. In this design, the PDN consists of a power conversion network (PCN) layer, power switch network (PSN) layer and a voltage regulator module (VRM). In PCN, the fixed outputs of VRM are used to generate all required voltage levels for various functional blocks in the system. PSN is used to connect the power supply terminal of each functional block dynamically to corresponding outputs of VRM in the PCN. An algorithm is used to select the best VRM's to achieve the design target of PDN. The proposed design is not only more power efficient but also reduces the cost of the PDN. The test results show that an average power reduction of 34% in PDN is possible with this approach. Also, an average of reduction in the cost of 8% can be achieved.

Woojoo et al. 2012 [55] propose three approaches to reduce the power consumption in smartphones. 1. profiling the power consumption of each module of the phone under different operating scenarios, 2. building an equivalent DC-DC converter (PDN) model for each smartphone module and estimate its power conversion efficiency, and 3. changing the parameters of the actual converters in the smartphone to improve the equivalent power conversion efficiencies for all modules. The experimental results show that we can achieve a power conversion efficiency 6% to 15% which translates up to 30% reduction in the

power losses incurred during power conversion in smartphones.

Woojoo et al. 2014 [56] present two optimization method; 1) maximizing the efficiency of a dc–dc converter under statistical loading profiles by static switch sizing and 2) achieving the high-efficiency enhancement under dynamically varying load conditions by dynamic switch modulation. The Experimental results demonstrate that the static switch sizing can contribute up to 6% power conversion efficiency enhancement, which translates to 19% reduction in power loss general usage of the smartphone.

6 ANALYSIS AND INFERENCE

In this paper, we reviewed several research papers concerning some commonly used power optimization techniques. The review of each paper was based on approaches, algorithms, equations, data, experimental results presented by the authors including their remarks, comments, and conclusions. The results of analysis are summarized in table 6.1. Only the percentage power saving opportunities concerning various techniques at different architectural, device and component levels using single or multiple techniques are shown in this table. Some of these techniques have an impact on performance, speed, area, and other constraints which are not shown here. The detailed review of these research papers revealed that most of the power reduction techniques hadbeen implemented for specific applications, specific devices, and specific components at different levels of abstraction in the system. Several techniques are available to optimize the power at different architecture levels; however, no single solution is there to address the power concerns of the entire system. These techniques are unique in terms of implementation - different solutions have been implemented and tested using different methodologies and different target platforms. Hence, itis difficult to compare these techniques and propose a best or an efficient solution.

TABLE 2
Percentage power saving opportunities

References	Techniques	Power Saving (Min)	Power saving (Max)
[11],[12]	Gate Sizing	10.00	15.50
[25]	Gate Sizing & Multi Threshold Voltage	0.00	30.00
[13]	Gate Sizing & Voltage Scaling	23.30	56.90
[14], [15],[16]	Logic Restructuring	19.00	57.00
[18]	Operand Isolation & Power gating	0.00	40.00
[17],[19]	Operand Isolation & Clock gating	25.00	40.00
[20],[22]	Body Biasing	43.00	50.00
[21]	Body Biasing & DVS	13.70	25.80
[23]	Multi Threshold Voltage & Multi Supply Voltage	0.00	38.10
[26],[27],[28]	Clock Gating	10.43	30.30
[30],[31],[32]	Memory Partitioning	30.00	80.00
[33],[34]	Bus Segmentation	0.00	60.00
[35],[36],[37]	Bus Encoding	46.00	63.00
[38],[39],[40]	Multi supply voltage	35.00	52.00
[41],[42],[43]	DVFS	11.39	52.23
[44],[45],[46],[47]	Power Gating	15.90	70.00
[48]	Power Gating, Multi threshold, Multi voltage	0.00	17.00
[49],[50],[51]	Hardware acceleration	29.00	55.00
[52],[53]	Selective Peripheral clocking	44.00	50.00
[54],[55],[56]	Configuring PDN& DVFS	19.00	34.05

7 CONCLUSION

Although a ton of techniques and solutions are proposed, the topic of power optimization in low power embedded systemsis still in the early stage as this area is being developed with advanced techniques at different abstraction levels. It is clear from the market trends that more advanced, faster and smarter portable devices with high computing density will be deployed in the future and hence the designers will also face more challenges for optimizing the power. Therefore, the researchers from the industrial world and academic community will have to put more efforts and come up with impressive research ideas to tackle the critical issue of optimizing the power consumption in low power embedded systems

In this paper, we analyzed various solutions concerning different power optimization techniques proposed by the research community in the recent years. We hope that this paper would help the researches in gaining a greater insight into the various power optmization techniques and propose effective solutions in designing the power-efficient low power embedded systems of tomorrow.

8 REFERENCES

[1] Sparsh Mittal: "A survey of techniques for improving energy efficiency in embedded computing systems", *International Journal of Computer Aided Engineering and Technology*, 6 (4), pp.440-459, 2014.

[2] R. Mendoza; A. Ferre; L. Balado; J. Figueras:"CMOS leakage power at cell level", IEEE *International Conference on Design and Test of Integrated Systems in Nano-scale Technology*, DTIS 2006, Year: 2006 Pages: 194 – 199, 2006.

[3] S. Borkar, "Low power design challenges for the decade", Proceedings of the ASP-DAC, IEEE Asia and South Pacific Design Automation Conference, Pages: 293 - 296, 2001

[4] Tadahiro Kuroda, " Low Power CMOS Design Challenges", *Invited paper, Special issue on Silicon Nano-devices, IEICE Trans. Electron*, Vol.E84-C, 2001

[5] Vasanth Venkatachalam, Michael Franz, "Power reduction techniques for microprocessor systems", *ACM Computing Surveys*, Vol. 37, No. 3, Pages 195–237, 2005

[6] Lubomir Valeriev Bogdanov, Racho Marinov Ivanov, "Approaches for reducing the power consumption in embedded systems", *Annual Jrnl. of Electronics*, ISSN 1314-0078, 2012.

[7] Srivaths Ravi, AnandRaghunathan, Paul Kocher, SunilHattangady; "Security inembedded systems: design challenges", *ACM transactions on embedded computingsystems, vol. 3, no. 3, August 2004, pages 461–491*

[8] S. Gupta et al., "Guaranteed QoS with MIMO Systems for Scalable Low Motion VideoStreaming Over Scarce Resource Wireless Channels," in Proceedings SecondInternational Conference On Information Processing, pp. 452–466, IK International PvtLtd, 2008.

[9] A. Munir, S. Ranka, and A. Gordon-Ross, "High performance energy-efficient multicoreembedded computing," IEEE Transactions on Parallel and Distributed Systems, vol. 23,no. 4, pp. 684–700, 2012.

[10] L. Smarr, "Project green light: Optimizing cyber infrastructure for a carbon-constrainedworld," Computer, vol. 43, no. 1, pp. 22–27, 2010.

[11] Wang; M. Olbrich; E. Barke; T. Büchner; M. Bühler; P. Panitz; "A gate sizing method for glitch power reduction" *IEEE International SOC Conference*, Pages: 24 - 29, 2011

[12] How-Rern Lin; Ting Ting Hwang "Power reduction by gate sizing with path-oriented slack calculation", *Design Automation Conference, Proceedings of the ASP-DAC '95/CHDL '95/VLSI '95., IFIP International Conference on HDL*,1995

[13] Chunhong Chen; M. Sarrafzadeh, "Power reduction by simultaneous voltage scaling and gate sizing",*Design Automation Conference. (IEEE Cat. No. 00CH37106)*, 2000.

[14] SenthilkumarJayapal, Janani SainathSigundey, Yipin Wu, and EricTTsai,"Stack effect and logic restructuring on high Fan-in FinFETs logic gates", *IEEE International Symposium on Integrated Circuits (ISIC)*, Pages: 1 – 4, 2016

[15] QuangDinh; Deming Chen; Martin D. F. Wong, "BDD-based circuit restructuring for reducing dynamic power" *IEEE Int. Conference on Computer Design*, Pages: 548 - 554, 2010

[16] Hosung (Leo) Kim, John Lillis, "A framework for layout-level logic restructuring",*Proceedings of the 2008 international symposium on Physical design, ACM*, 2008

[17] Jun Chao; Yixin Zhao; Zhijun Wang; Songping Mai; Chun Zhang, "Low-power implementations of DSP through operand isolation and clock gating", 2007 7th International Conference on ASIC Year: 2007 Pages: 229 - 232

[18] N. Banerjee; A. Raychowdhury; K. Roy; S. Bhunia; H. Mahmoodi, " Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Volume: 14, 2006.

[19] FábioLuísLivi Ramos; Jones Goebel; Bruno Zatt; Marcelo Porto; Sergio Bampi "Low-power hardware design for the HEVC Binary Arithmetic Encoder targeting 8K videos." *29th Symposium on Integrated Circuits and Systems Design*, Pages: 1 - 6, Year: 2016

[20] A. Youssef, M. Anis, and M. Elmasry, "Leakage control for large fan-in Domino gates using substrate biasing", *Proceedings of the 12th IEEE International Conference on Fuzzy Systems* (Cat. No.03CH37442) Pages: 81 - 84, 2003

[21] Po-Kuan Huang, and S. Ghiasi, "Power-Aware Compilation for Embedded Processors with Dynamic Voltage Scaling and Adaptive Body Biasing Capabilities", *Proceedings of the Design Automation & Test in Europe Conference*, Vol. 1 Page: 1 - 2, 2006

[22] Seidai Takeda, Shinobu Miwa, KimiyoshiUsami, and Hiroshi Nakamura, "Stepwise sleep depth control for run-time leakage power saving", *GLSVLSI '12: ACM Proceedings of the great lakes symposium on VLSI*, May 2012

[23] Gufran Ahmad; Yogesh Kumar; Praveen Kumar Sahu "High performanceMulti Threshold voltage level converter for multi-VDD systems", IEEE *Students Conference on Engineering and Systems (SCES), pages*: 1 - 4, 2013

[24] Frank Sill, Frank Grassert, Dirk Timmermann, "Low power gate-level design with mixed-Vth (MVT) techniques", SBCCI '04: *Proceedings of the 17th symposium on Integrated circuits and system design Publisher: ACM*, September 2004

[25] Feng Gao; J. P. Hayes, "Total power reduction in CMOS circuits via gate sizing and multiple threshold voltages", *Proceedings. 42nd Design Automation Conf.*, 2005.

[26] M. Maria Dominic Savio; M. Arokia Mary "A clock tree based gated driver in low power delay buffer" *International Conference on Electrical, Electronics, and Optimization Techniques* (ICEEOT) Pages: 4767 - 4772, Year: 2016

[27] PritamBhattacharjee; AlakMajumder; TusharDhabal Das, "A 90 nm leakage control transistor based clock gating for low power flip flop applications", *IEEE 59th Int.l Midwest Symposium on Circuits and Systems*, Pages: 1 - 4, 2016

[28] DoronGluzer; Shmuel Wimer "Probability-Driven Multibit Flip-Flop Integration With Clock Gating" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Volume: 25, Issue: 3 Pages: 1173 -1177, Year: 2017.

[29] Jie Li; Xing Wan; Jianbing Wu; Weiwei Shan "Cache Power Optimization Based on Compare-Based Adaptive ClockGating and Its 65nm SoC Implementation", *Chinese Journal of Electronics*, Vol. 26, Issue: 1 Pages: 128 - 131, 2017.

[30] Mathew Paul; Peter Petrov, "Dynamically Adaptive I-Cache Partitioning for Energy Efficient Embedded Multitasking", *IEEE Transactions on VLSI Systems,* Volume: 19, Issue: 11 Pages: 2067 -2080, IEEE Journals & Magazines, ear: 2011,

[31] Alice M. Tokarnia; Marina Tachibana "Design of Trace-Based Split Array Caches for Embedded Applications" 2010 13th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, Pages: 21 - 27, Year: 2010

[32] Jason Cong; Wei Jiang; Bin Liu; Yi Zou, "Automatic memory partitioning and scheduling for throughput and power optimization" *IEEE/ACM International Conference on Computer-Aided Design - Digest of Technical Papers,* Year: 2009.

[33] Hua Wang, AntonisPapanikolaou, Miguel Miranda, FranckyCatthoor, "A global bus power optimization methodology for physical design of memory dominated systems by coupling bus segmentation and activity driven block placement", *Proc. of the Asia and South Pacific Design Automation Conf.* IEEE Press, 2004.

[34] Suresh Srinivasan, Lin Li, N. Vijaykrishnan, "Simultaneous Partitioning and Frequency Assignment for On-Chip Bus Architectures", Proc. of the conf. on Design, Automation and Test in Europe – Vol.1, IEEE Computer Society, 2005.

[35] Dinesh C. Suresh, Banit Agrawal, Jun Yang, WalidNajjar, LaxmiBhuyan, "Power efficient encoding techniques for off-chip data buses", *Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems,* ACM, October 2003

[36] Shidi Qu; Young-ChulKimA, "new power aware bus encoding scheme for system on a chip" *IEEE 15th Int. Sym.on Consumer Electronics*, Pages: 416 - 420, 2011

[37] P Mohammad Hossein Hajkazemi; MisaghTakapoo; Mohammad BagherGhaznavi-Ghoushchi, "ABEM: A new power-aware adaptive bus encoding method using Huffman algorithm*", IEEE International Symposium on Computer Networks*

[38] Anish Muttreja; Prateek Mishra; Niraj K. Jha, "Threshold Voltage Control through Multiple Supply Voltages for Power-Efficient FinFET Interconnects" *IEEE 21st International Conference on VLSI Design,* Pages: 220 - 227, 2008

[39] Marco Terres, Cristina Meinhardt, GuilhermeBontorin, andRicardo Reis, "A novel approach to reduce power consumption in level shifter for Multiple Dynamic Supply Voltage",*IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS),* Pages: 715 - 718, 2013.

[40] Harry Kalargaris; John Goodacre; Vasilis F. Pavlidis, "Advanced circuit interface for systems with multiple voltage domains", *12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME),* Pages: 1 - 4, 2016

[41] Ying-Xun Lai; Yueh-Min Huang; Chin-Feng Lai; LjiljanaTrajkovic, "Parallel Dynamic Voltage and Frequency Scaling for stream decoding using a multicore embedded system",*IEEE Int. Symp. of Circuits and Systems*, 2016.

[42] Changyi Deng; RuifengGuo; Hongliang Wang; Azhen Peng, "A Dynamic Power Management Algorithm for Sporadic Tasks in Real-Time Embedded Systems" *IEEE Trustcom/BigDataSE/ISPA*, Pages: 2073 - 2078, 2016

[43] AnasToma; Santiago Pagani; Jian-Jia Chen; Wolfgang Karl; JörgHenkel "An Energy-Efficient Middleware for Computation Offloading in Real-Time Embedded Systems": *IEEE 22nd International Conference on Embedded and Real-Time Computing Systems and Applications,* Pages: 228 - 237, 2016.

[44] Ricardo Gomez, Flavius Gruian, Liang Liu, "Memory Power Management for Java Processors Using Heap Partitioning and Power Gating",*Proceedings of the 14th Intl. Workshop on Java Technologies for Real-Time & Embedded systems*, ACM, 2016

[45] Ye-Jyun Lin, Chia-Lin Yang, Jiao-We Huang, Tay-Jyi Lin, Chih-Wen Hsueh, Naehyuck Chang "System-Level Performance and Power Optimization for MPSoC A Memory Access-Aware Approach" *ACM Transactions on Embedded Computing Systems:* 2015

[46] Michael Henry, MeetaSrivastav, Leyla Nazhandali, "A case for NEMS-based functional-unit power gating of low-power embedded microprocessors" Proceedings of the 48th Design Automation Conference, ACM, 2011

[47] Rahul Boyapati, Jiayi Huang, Ningyuan Wang, Kyung Hoon Kim, Ki Hwan Yum, Eun Jung Kim,PPOSTER: Fly-Over: "A Light-Weight Distributed Power-Gating Mechanism For Energy-Efficient Networks-on-Chip" ACM *Proceedings of the Int. Conference on Parallel Architectures and Compilation,*2016

[48] VazgenMelikyan; Tigran akhverdyan; Sergeyanukyan; Aram Gevorgyan; Davit Babayan, "Low power Open RISC processor with power gating, multi-VTH and multi-voltage techniques" , IEEE East-West Design & Test Symposium, 2012

[49] Giuseppe Tagliavini; GermainHaugou; Andrea Marongiu; Luca Benini "Enabling OpenVX support in mW-scale parallel accelerators" International Conference on Compliers, Architectures, and Sythesis of Embedded Systems, Pages: 1-10, 2016

[50] Renzo Andri; Lukas Cavigelli; Davide Rossi; Luca Benini "YodaNN: An Ultra-Low Power Convolutional Neural Network Accelerator Based on Binary Weights", *IEEE Comp. Society Annual Symposium on VLSI*, 2016

[51] Altera Corporation, "Adding Hardware Accelerators to Reduce Power in Embedded Systems" *White paper*, 2009.

[52] OzgurCelebican, TajanaSimunicRosing, Vincent J. Mooney, IIIEnergy estimation of peripheral devices in embedded systems, *Proceedings of the 14th ACM Great Lakes symposium on VLSI*, GLSVLSI '04, 2004

[53] Andrea Acquaviva1, TajanaSimunic, Vinay Deolalikar, Sumit Roy, "Server Controlled Power Management for Wireless Portable Devices, Mobile and Media Systems Laboratory", *HP Laboratories Palo Alto*, HPL-2003-82, 2003

[54] Behnam Amelifard, MassoudPedram, "Design of an efficient power delivery network in an soc to enable dynamic power management", *Proceedings of the 2007 international symposium on Low power electronics and design*, 2007

[55] Woojoo Lee, Yanzhi Wang, Donghwa Shin, Naehyuck Chang, MassoudPedram, "Power conversion efficiency characterization and optimization for smartphones" *Proceedings of the ACM/IEEE international symposium on Low power electronics and design, 2012.*

[56] Woojoo Lee, Yanzhi Wang, Donghwa Shin, Member, Naehyuck Chang, and MassoudPedram, "Optimizing the

Power Delivery Network in a Smartphone Platform", *IEEE Tran. on computer-aided design of integrated circuits and systems,* VOL. 33, 2014.

[57] Mark P. Mills, "The cloud begins with coal: Big data, Big networks, Big infrastructure, and Big power – An overview of the electricity used by the global digital ecosystem",*https:/www.tech-pundit.com*, August 2013.

[58] D. Anderson, J. Dykes, and E. Riedel, "More than an interface-SCSI vs. ATA," *in 2nd USENIX Conference on File and Storage Technologies* (FAST03), pp. 245–257, 2003.

[59] Chong-Min Kyung, SungjooYoo , "Energy-Aware System Design Algorithms and Architectures", 978-94-007-1679-7 (Online), Springer, 2011

[60] A. Nazarudeen and P. Jayaprakash, "A Review of Techniques for Power Optimization at Different Levels of Abstraction of Low Power Embedded Systems", Accepted for publication in *International Journal of Application or Innovation in Engineering & Management (IJAIEM),* ISSN 2319 – 4847, *Volume 6, Issue 6*, June 2017.